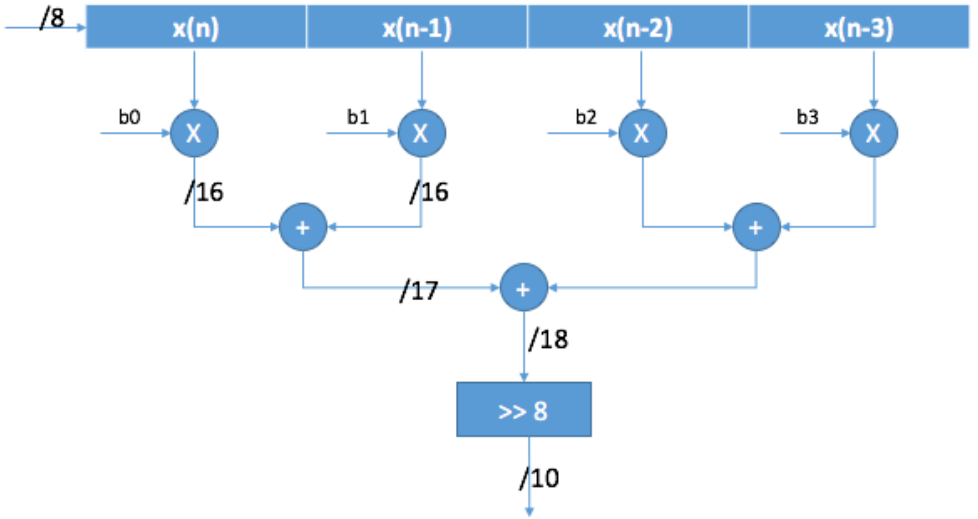
Mastering DSP in VHDL

- Fixed point arithmetic ➔ complex VHDL design using Digital signal processing
- Digital filtering
- C++
- Matlab
- Signal Theory



Mastering DSP in VHDL

- Mandatory VHDL Syntax ➔

Start Learning VHDL using FPGA

- Write to: info@surf-vhdl.com

Mastering DSP in VHDL - Section 1

- continuous-time signal
- discrete-time signal
- Time domain and Frequency domain representation
- Function $\delta(n)$ and u(n)
- Analog to Digital and Digital to Analog Conversion
- Quantization error, SRN, SINAD

Mastering DSP in VHDL - Section 2

- Introduction to Digital Filter Design
- Example of Mobile Average Filter
- FIR general architecture
- Frequency response
- Impulse response
- Step response
- MATLAB/C++ implementation
    - Symmetric FIR
    - Antisymmetric FIR
    - Half-Band FIR

Mastering DSP in VHDL - Section 3

- ☞ Introduction to Fixed point arithmetic
- ☞ Floating point -> Fixed point
- ☞ Fixed point representation
- ☞ Add, Sub, Mult, Acc

Mastering DSP in VHDL - Section 4

- Filter synthesis using Matlab/Octave
- Filter design example using the Matlab Remez function to synthesize a digital filter
- Fixed point verification Matlab/Octave/C++

Mastering DSP in VHDL - Section 5

- VHDL implementation of Mobile Average Filter
- VHDL implementation of classic FIR
- VHDL implementation of a symmetric FIR
- VHDL implementation of an antisymmetric FIR

Mastering DSP in VHDL - Section 6

- Introduction to multi-rate filter
- Interpolation
- FIR Interpolator
- Decimation
- FIR Decimation
- Fractional interpolation/Decimation

Mastering DSP in VHDL - Section 7